REMARKS/ARGUMENTS

Claims 1-13 are pending in this application. By this Amendment, Applicant amends claims 1 and 8 and cancel claims 14-16.

Applicant affirms the election of Group I including claims 1-13 without traverse. Claims 14-16 have been canceled since these claims are directed to a non-elected invention. Applicant reserves the right to file a Divisional Application to pursue prosecution of non-elected claims 14-16.

Claims 1-13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hosoya (JP 8-340213) in view of Nakamura et al. (U.S. 5,438,218). Applicant respectfully traverses this rejection.

Claim 1 has been amended to recite:

> "A semiconductor device comprising:
> a semiconductor substrate;
> a field effect transistor provided on the semiconductor substrate and having electrodes, the field effect transistor having a gate recess and a Schottky junction for a gate electrode;
> a pn junction diode provided on the semiconductor substrate and having electrodes, the pn junction diode having an n-type layer and a p-type layer; and
> **at least one ion implanted region disposed between the field effect transistor and the pn junction diode**; wherein
> at least one of the electrodes of the field effect transistor and at least one of the electrodes of the pn junction diode are composed of metal conductors which are simultaneously formed." (emphasis added)

Applicant's claim 8 recites features that are similar to the features recited in Applicant's claim 1, including the above-emphasized features.

With the unique combination and arrangement of elements recited in Applicant's claims 1 and 8, including the feature of "at least one ion implanted region disposed between the field effect transistor and the pn junction diode," Applicant has been able to provide a semiconductor device in which the region where the field effect transistor is provided and the region the pn junction diode is provided are separated from one

another by the ion implanted region, such that the field effect transistor and the pn junction diode can be simultaneously formed, which simplifies the process of manufacturing of the semiconductor device and reduces the cost thereof (see, for example, the third full paragraph on page 4 and the fifth and sixth full paragraphs on page 10 of the originally filed specification).

The Examiner alleged that Hosoya teaches all of the features recited in Applicant's claims 1 and 8, except for a diode that is a pn junction diode having a p-type layer and an n-type layer. The Examiner further alleged that Nakamura et al. teaches this feature. Thus, the Examiner concluded that it would have been obvious "to modify the invention of Hosoya with the pn diode having a p-type layer and an n-type layer, as taught by Nakamura, so as to improve the breakdown voltage of the diode."

Applicant's claims 1 and 8 have been amended to recite the feature of "at least one ion implanted region disposed between the field effect transistor and the pn junction diode."

Neither Hosoya nor Nakamura et al. teaches or suggests <u>any</u> ion implanted regions. Thus, Hosoya and Nakamura et al. certainly fail to teach or suggest the feature of "at least one ion implanted region disposed between the field effect transistor and the pn junction diode" as recited in Applicant's claims 1 and 8.

Accordingly, Applicant respectfully submits that Hosoya and Nakamura et al., applied alone or in combination, fail to teach or suggest the unique combination and arrangement of elements recited in Applicant's claims 1 and 8.

Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 1 and 8 under 35 U.S.C. § 103(a) as being unpatentable over Hosoya and Nakamura et al.

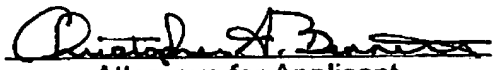
In view of the foregoing amendments and remarks, Applicant respectfully submits that Claims 1 and 8 are allowable. Claims 2-7 and 9-13 depend upon claims 1 and 8, and are therefore allowable for at least the reasons that claims 1 and 8 are allowable.

In view of the foregoing amendments and remarks, Applicants respectfully submit that this application is in condition for allowance. Favorable consideration and prompt allowance are solicited.

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

Date: April 1, 2005



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